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10/061,504	02/01/2002	Robert M.R. Neff	10010205-1	2083

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EXAMINER
NGUYEN, LINH M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/061,504	NEFF, ROBERT M.R.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 02/01/2002 is in compliance with the provisions of 37 CFR 1.97 and 1.98. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to because of the following informalities:

(i) lacking Prior Art labels in figures 1A, 1B, 2A, 2B, 3A, and 3B; and

(ii) failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "10" in line 16 of page 1; and "K0" in line 3 of page 11.

Correction is required.

3. Figures 1A, 1B, 2A, 2B, 3A, and 3B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (according to paragraphs [0003-0028] of the disclosure of the instant application). See MPEP § 608.02(g).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Correction is required.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

Line 11, replace "clock signal generator" with -- clock generator --, to be consistent with line 8.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 1, 6-8, 10-13, 16-17, and 19-20, the parameters "M, N, and N/M" recited therein render the claims indefinite as there is no numerical value(s) or range(s) provided to define what they are. It appears that both N and M are integers greater than 1, and that N is a multiple of M. If the interpretation is correct, providing such an informative support is suggested. Explanation is required.

Claims 2-5, 9, 14, and 18 are also rejected due to their dependency on claims 1 and 13.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 9-11, 13, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Betts (U.S. Patent No. 4,430,745).

With respect to claim 1, as best understood, Betts discloses, in Figure 2, an interleaved clock generator for generating N (N=3 in this case) interleaved clock signals [CK1, CK2, CK3] in response to an input clock signal [TC]; the interleaved clock generator comprises (1) interleaved clock generator means of a first type which includes a ring counter circuit [3, 48, 49] *(see col. 4, line30)*, for (i) receiving the input clock signal [TC], and (ii) generating in response thereto M *(M=3 in this case)* interleaved intermediate clock signals *[outputs from terminals Q of [3, 48, 49] and inputs to [5, 33, 35]]*, and (2) M (M=3 in this case) interleaved clock generator means of a second type [5 & 7, 33 & 34, 35 & 36], which are configured for (i) receiving a respective one of the intermediate clock signals *[outputs from [3, 48, 49] and inputs to [3, 33, 35]]* from the clock generator means of the first type, and (ii) generating in response thereto N/M *(N/M =3/3 in this case)* of the N *(N=3 in this case)* interleaved clock signals; wherein each of the interleaved clock signal generator means of the second type includes a multi-stage serial-delay circuit *(formed by a pair of drivers/delay elements [5 & 7, 33 & 34, 35 & 36])*.

With respect to claim 9, Betts discloses, in Figure 2, that (1) the interleaved clock generator means of the first type includes the ring counter circuit [3, 48, 49] (see col. 4, line 30), and (2) each of the interleaved clock signal generator means of the second type includes the multi-stage serial-delay circuit [5 & 7, 33 & 34, or 35 & 36].

With respect to claim 10, as best understood, Betts discloses, in Figure 2, that the ring counter circuit [3, 48, 49] includes an M-stage *(M=3 in this case)* ring counter.

With respect to claim 11, as best understood, Betts discloses, in Figure 2, that (1) the multi-stage serial-delay circuit includes N/M delay stages (N=3 and M=3; N/M=3/3 in this case), and (2) each of the stages provides one of the interleaved clock signals [CK1, CK2, or CK3].

With respect to claim 13, as best understood, Betts discloses, in Figure 2, an interleaved clock generator for generating N (N=3 in this case) interleaved clock signals [CK1, CK2, CK3] in response to an input clock signal [TC]; the interleaved clock generator comprises (1) an interleaved clock generator of a first type, which includes (i) a ring counter circuit [3, 48, 49] *(see col. 4, line30)*, (ii) a clock input [CK] for receiving the input clock signal [TC], and (iii) M (M=3 in this case) intermediate clock outputs *(from terminals Q of [3, 48, 49])*, for operating in response to the input clock signal [TC] to output a respective intermediate clock signal at each of the intermediate clock outputs *(from terminals Q of [3, 48, 49])*, and (2) M (M=3 in this case) interleaved clock generators of a second type [5 & 7, 33 & 34, 35 & 36], which individually include (i) an intermediate clock input connected to a different one of the M intermediate clock outputs of the interleaved clock signal generator of the first type [3, 48, 49], (ii) N/M *(N/M=3/3 in this case)* clock outputs, and (iii) the multi-stage serial-delay circuit; wherein each of the interleaved clock generators of the second type operates in response to the intermediate clock signal to output a respective one of N/M of the interleaved clock signals at each of the clock outputs.

With respect to claim 18, Betts discloses, in Figure 2, that (1) the interleaved clock generator of the first type includes the ring counter circuit [3, 48, 49] (see col. 4, line 30), and (2) each of the interleaved clock signal generator means of the second type includes the multi-stage serial-delay circuit [5 & 7, 33 & 34, or 35 & 36].

With respect to claims 19 and 20 as best understood, Betts discloses, in Figure 2, an interleaved clock generator for generating N *(N=3 in this case)* interleaved clock signals [CK1, CK2, CK3] in response to an input clock signal [TC]; the interleaved clock generator comprises

(1) a multi-stage serial-delay circuit [5 & 7, 33 & 34, 35 & 36], including M *(M=3 in this case)* intermediate clock outputs *(or inputs of [5, 33, 35])*, connected to receive the input clock signal [TC], and (2) a ring counter circuit [3, 48, 49] *(see col. 4, line30)* connected to each of the M *(M=3 in this case)* intermediate clock outputs *(inputs of [5, 33, 35])* for generating N/M *(N/M=3/3 in this case)* of the N interleaved clock signals [outputs from terminals Q of elements 3, 48, 49]; wherein the ring counter circuit includes an N/M-stage ring counter *(N/M = 3/3=1 in this case)*.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-3, 5-7, 13, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dally et al. (U.S. Patent No. 6,275,072), in view of Muscavage (U.S. Patent No. 5,268,656).

With respect to claims 1 and 5-6, as best understood, Dally et al. discloses, in Fig. 2, a clock generator comprising interleaved clock generator means of a first type [121-125, 126, 127, 128, 130, 129] *(in this case, it is a multi-stage serial-delay circuit since it is configured with delay elements)*] for (i) receiving the input clock signal [aclk], and ii) generating in response thereto M *(M=number of intermediate of clock signals=4 in this case)* intermediate clock signals [bclk, cclk, dclk, eclk]; wherein the interleaved clock generator means of the first type includes a multi-stage serial-delay circuit [121,..., 130 *(delay elements, inverters)*].

Dally et al.'s teachings lack M interleaved clock generator means of a second type, which individually include a ring counter circuit, for (i) receiving a respective one of the intermediate clock signals from the clock generator means of the first type, and ii) generating in response thereto N/M of N interleaved clock signals; wherein the ring counter circuit includes an N/M-stage ring counter.

Muscavage discloses, in Fig. 2, a clock generator comprising M *(M=4 in this case)* interleaved clock generator means of a second type, which individually include a ring counter circuit [30, 32, 34, or 36], for (i) receiving a respective one of the intermediate clock signals from the clock generator means of the first type, and ii) generating in response thereto N/M *(N/M = 32/4 in this case)* of N *(N=32 in this case)* interleaved clock signals *(N=32 is the number of outputs from 4 ring counters [30, 32, 34, and 36]; each counter generates 8 output clock signals; for example, ring counter [30] generates 8 outputs from 8 flip-flops [0, 4, 8, 12, 16, 20, 24, and 28]);* wherein the ring counter circuit includes an N/M-stage ring counter *(N/M = 32/4 = 8, which is the number of ring counters/flip-flops; for example, ring counter [30] is configured with 8 flip-flops [0, 4, 8, 12, 16, 20, 24, and 28]).*

To implement the clock generator system of Dally et al. by additionally arranging a number of clock generators including a corresponding number of ring counter circuits configured with N/M ring counters therein for a generation of multiple phases of a desired clock signal would have been obvious to one of ordinary skill in the art at the time of the invention since such an arrangement of clock generators with ring counter circuits for the stated purpose has been a well-known practice in the art as evidenced by the teachings of Muscavage (see Muscavage; col. 2, lines 1-2).

With respect to claim 2, Dally et al. discloses, in Fig. 2, that the multi-stage serial-delay circuit includes a delay-locked loop *(Fig. 2 of Dally et al. shows a delay-locked loop having a delay line with delay elements and inverters [121-125]; once the delayed-locked loop has converged, [bclk] and [fclk] are in phase (col. 1, line 23-25)).*

With respect to claim 3, Dally et al. discloses, in Fig. 2, that the multi-stage serial-delay circuit includes a phase-locked loop *(Fig. 2 of Dally et al. shows a phase-locked loop with a phase comparator [126]; the phase comparator compares phases [bclk] and [fclk] and outputs control signals up and down to charge pump to adjust the voltage on the inverter supply line [129] to bring [bclk] and [fclk] in phase (col. 1ines 17-19 and 21-23)).*

With respect to claims 7 and 17, Dally et al. discloses, in Fig. 2, that (i) the multi-stage serial-delay circuit [121,...,130] includes M delay stages [121-124] *(M = 4 in this case)*, and (2) each stage provides one of the intermediate clock signals [bclk, cclk, dclk, eclk].

With respect to claims 13, 15, and 16, as best understood, Dally et al. discloses, in Fig. 2, a clock generator comprising an interleaved clock generator of a first type [121-125, 126, 127, 128, 130, 129] (*in this case, it is a multi-stage serial-delay circuit since it is configured with delay elements)*] for (i) receiving the input clock signal [aclk], and ii) generating in response thereto M *(M=number of intermediate of clock signals=4 in this case)* intermediate clock signals [bclk, cclk, dclk, eclk]; wherein the interleaved clock generator of the first type includes a multi-stage serial-delay circuit [121,..., 130 *(delay elements, inverters)*].

Dally et al.'s teachings lack M interleaved clock generators of a second type, which individually include a ring counter circuit, for (i) receiving a respective one of the intermediate clock signals from the clock generators of the first type, and ii) generating in response thereto

N/M of N interleaved clock signals; wherein the ring counter circuit includes an N/M-stage ring counter.

Muscavage discloses, in Fig. 2, a clock generator comprising M *(M=4 in this case)* clock generators of a second type, which individually include a ring counter circuit [30, 32, 34, or 36], for (i) receiving a respective one of the intermediate clock signals from the clock generator means of the first type, and ii) generating in response thereto N/M *(N/M = 32/4 in this case)* of N *(N=32 in this case)* interleaved clock signals *(N=32 is the number of outputs from 4 ring counters [30, 32, 34, and 36]; each counter generates 8 output clock signals; for example, ring counter [30] generates 8 outputs from 8 flip-flops [0, 4, 8, 12, 16, 20, 24, and 28]);* wherein the ring counter circuit includes an N/M-stage ring counter *(N/M = 32/4 = 8, which is the number of ring counters/flip-flops; for example, ring counter [30] is configured with 8 flip-flops [0, 4, 8, 12, 16, 20, 24, and 28]).*

To implement the clock generator system of Dally et al. by additionally arranging a number of clock generators including a corresponding number of ring counter circuits configured with N/M ring counters therein for a generation of multiple phases of a desired clock signal would have been obvious to one of ordinary skill in the art at the time of the invention since such an arrangement of clock generators with ring counter circuits for the stated purpose has been a well-known practice in the art as evidenced by the teachings of Muscavage (see Muscavage; col. 2, lines 1-2).

Allowable Subject Matter

11. Claims 4, 8, 12, and 14 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112 set forth in this Office Action and to include all of the limitations of the base claims and any intervening claims.

Prior art of record does not show or fairly suggest:

(i) A specific frequency of the interleaved clock signals and that of the input clock signal; wherein (a) for the interleaved clock signals, the frequency is 1/ (N x Td), and (b) for the input clock signal, (b_1) the frequency is 1/ (M x Td) when the interleaved clock generator means of the first type includes the multi-stage serial delay means, and (b_2) the frequency is M/ (N x Td) when the interleaved clock generator means of the first type includes the ring counter circuit, as called for in claims 4 and 14; and

(ii) An interleaved clock signal generator, in which (a) the input clock signal comprises differential clock signals, (b) each of the differential clock signals has 50% duty cycle, (c) the multi-stage serial-delay circuit includes M/2 delay stages, and (d) each of the delay stages provides two of the intermediate clock signals, as called for in claims 8 and 12.

Citation of Relevant Prior Art

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Kusumoto et al. (U.S. Patent No. 5,828,717) discloses a counting circuit for measuring time as the pulse spacing of a pulse signal.

Prior art Ihara et al. (U.S. Patent No. 5,371,773) discloses a counter circuit including counting stages of n bits.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and (703) 305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Linh M. Nguyen
Examiner
Art Unit 2816

LMN
October 17, 2002